

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:
- a shielding film formed on an insulating surface;
  - a planarization insulating film formed on the insulating surface so as to
  - 5 cover the shielding film; and
  - a semiconductor layer formed so as to be in contact with the planarization insulating film,
  - wherein the shielding film overlaps the semiconductor layer with the planarization insulating film sandwiched therebetween, and
  - 10 wherein the planarization insulating film is polished by CMP before the semiconductor layer is formed.
2. A device according to claim 1, wherein a thickness of the shielding film is 0.1  $\mu\text{m}$  to 0.5  $\mu\text{m}$ .
3. A device according to claim 1, wherein the shielding film is tapered around the edge.
4. A digital camera comprising a semiconductor device according to claim 1.
5. A video camera comprising a semiconductor device according to claim 1.
6. A goggle type display device comprising a semiconductor device according to claim 1.
7. An audio system comprising a semiconductor device according to claim 1.

8. A notebook personal computer comprising a semiconductor device according to claim 1.

9. A portable information terminal comprising a semiconductor device according to claim 1.

10. A DVD player comprising a semiconductor device according to claim 1.

11. A semiconductor device comprising:

10 a shielding film formed on an insulating surface;

a planarization insulating film formed on the insulating surface so as to cover the shielding film; and

a thin film transistor including an active layer, the transistor being formed so as to be in contact with the planarization insulating film,

15 wherein the active layer has a channel formation region,

wherein the shielding film overlaps the entire channel formation region with the planarization insulating film sandwiched therebetween, and

wherein the planarization insulating film is polished by CMP before the active layer is formed.

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12. A device according to claim 11, wherein a thickness of the shielding film is 0.1  $\mu\text{m}$  to 0.5  $\mu\text{m}$ .

13. A device according to claim 11, wherein the shielding film is tapered around the edge.

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14. A digital camera comprising a semiconductor device according to claim 11.

15. A video camera comprising a semiconductor device according to claim 11.

16. A goggle type display device comprising a semiconductor device according to claim 11.

17. An audio system comprising a semiconductor device according to claim 11.

18. A notebook personal computer comprising a semiconductor device according to claim 11.

19. A portable information terminal comprising a semiconductor device according to claim 11.

20. A DVD player comprising a semiconductor device according to claim 11.

21. A semiconductor device comprising:  
a lower layer capacitance wiring formed on an insulating surface;  
a planarization insulating film formed on the insulating surface so as to cover the lower layer capacitance wiring; and  
a capacitance wiring formed so as to be in contact with the planarization insulating film,



29. A notebook personal computer comprising a semiconductor device according to claim 21.

30. A portable information terminal comprising a semiconductor device according to claim 21.

31. A DVD player comprising a semiconductor device according to claim 21.

32. A semiconductor device comprising:

10 a shielding film, a lower layer capacitance wiring and a lower layer wiring that are formed on an insulating surface;

a planarization insulating film formed on the insulating surface so as to cover the shielding film, the lower layer capacitance wiring and the lower layer wiring;

15 a thin film transistor including an active layer, the transistor being formed so as to be in contact with the planarization insulating film; and

a capacitance wiring formed so as to be in contact with the planarization insulating film,

wherein the active layer has a channel formation region,

20 wherein the shielding film overlaps the entire channel formation region with the planarization insulating film sandwiched therebetween,

wherein the lower layer capacitance wiring overlaps the capacitance wiring with the planarization insulating film sandwiched therebetween,

25 wherein the thin film transistor has a gate electrode electrically connected to the lower layer wiring, and

wherein the planarization insulating film is polished by CMP before the active layer is formed.

33. A device according to claim 32, wherein the shielding film, the lower layer  
5 capacitance wiring and the lower layer wiring each has a thickness of 0.1  $\mu\text{m}$  to 0.5  $\mu\text{m}$ .

34. A device according to claim 32, wherein the shielding film, the lower layer  
capacitance wiring and the lower layer wiring are tapered around their edges.

10 35. A device according to claim 32, wherein the thickness of the planarization  
insulating film is 0.5  $\mu\text{m}$  to 1.5  $\mu\text{m}$ .

15 36. A digital camera comprising a semiconductor device according to claim  
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37. A video camera comprising a semiconductor device according to claim 32.

20 38. A goggle type display device comprising a semiconductor device according  
to claim 32.

39. An audio system comprising a semiconductor device according to claim  
32.

25 40. A notebook personal computer comprising a semiconductor device according

to claim 32.

41. A portable information terminal comprising a semiconductor device according to claim 32.

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42. A DVD player comprising a semiconductor device according to claim 32.

43. A method of manufacturing a semiconductor device, comprising the steps of:

10 forming a shielding film that is in contact with an insulating surface;  
forming an insulating film on the insulating surface so as to cover the shielding film;  
polishing the insulating film by CMP to form a planarization insulating film;  
and  
15 forming a semiconductor layer such that it is in contact with the planarization insulating film,  
wherein the shielding film overlaps the semiconductor layer with the planarization insulating film sandwiched therebetween.

20 44. A method according to claim 43, wherein the thickness of the shielding film is 0.1  $\mu\text{m}$  to 0.5  $\mu\text{m}$ .

45. A method according to claim 43, wherein the shielding film is tapered around the edge.

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46. A method according to claim 43, wherein the thickness of the planarization insulating film is 0.5  $\mu\text{m}$  to 1.5  $\mu\text{m}$ .

47. A method of manufacturing a semiconductor device, comprising the steps  
5 of:

forming a shielding film that is in contact with an insulating surface;

forming an insulating film on the insulating surface so as to cover the shielding film;

polishing the insulating film by CMP to form a planarization insulating film;

10 and

forming a thin film transistor including an active layer such that it is in contact with the planarization insulating film,

wherein the active layer has a channel formation region, and

wherein the shielding film overlaps the entire channel formation region with  
15 the planarization insulating film sandwiched therebetween.

48. A method according to claim 47, wherein the thickness of the shielding film is 0.1  $\mu\text{m}$  to 0.5  $\mu\text{m}$ .

20 49. A method according to claim 47, wherein the shielding film is tapered around the edge.

50. A method according to claim 47, wherein the thickness of the planarization insulating film is 0.5  $\mu\text{m}$  to 1.5  $\mu\text{m}$ .

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wiring that are in contact with an insulating surface;

forming an insulating film on the insulating surface so as to cover the shielding film, the lower layer capacitance wiring and the lower layer wiring;

polishing the insulating film by CMP to form a planarization insulating film;

5 and

forming a capacitance wiring and a thin film transistor that includes an active layer on the planarization insulating film,

wherein the active layer has a channel formation region,

wherein the shielding film overlaps the entire channel formation region with

10 the planarization insulating film sandwiched therebetween,

wherein the lower layer capacitance wiring overlaps the capacitance wiring with the planarization insulating film sandwiched therebetween, and

wherein the thin film transistor has a gate electrode electrically connected to the lower layer wiring.

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56. A method according to claim 55, wherein the shielding film, the lower layer capacitance wiring and the lower layer wiring each has a thickness of 0.1  $\mu\text{m}$  to 0.5  $\mu\text{m}$ .

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57. A method according to claim 55, wherein the shielding film, the lower layer capacitance wiring and the lower layer wiring are tapered around their edges.

58. A method according to claim 55, wherein the thickness of the planarization insulating film is 0.5  $\mu\text{m}$  to 1.5  $\mu\text{m}$ .

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